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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,310	09/26/2003	Akira Ishikawa	740756-2654	5329

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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 08/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/670,310	ISHIKAWA, AKIRA	
	Examiner	Art Unit	
	Lex Malsawma	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Sep. 26, 2003 through Jan. 16, 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *17-20* is/are allowed.

6)☒ Claim(s) *1-16,21-23 and 25* is/are rejected.

7)☒ Claim(s) *24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20030926, 20040116*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2 and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by Borel et al. (6,297,093 B1; hereinafter, "**Borel**").

Regarding claims 1, 2 and 4:

Borel discloses (in Figs. 2A-2C and Col. 2, lines 30-62) a semiconductor device manufacturing method, comprising the steps of:

forming a semiconductor film on a substrate, i.e., Borel discloses forming "the cell" in an active area of the substrate (Col. 2, lines 23-29); the active area would at least be a semiconductor region on the substrate; therefore, the active area could be referred to as a semiconductor film on the substrate;

forming a gate insulating film 3 on the semiconductor film;

forming a gate electrode 4 on the gate insulating film 3;

adding a first impurity 11 to the semiconductor film while using the gate electrode 4 as a mask (Col. 2, lines 34-36);

forming a conductive film 21 over the gate insulating film and the gate electrode;

forming a sidewall 23/24 to a side surface of the gate electrode in a condition of the gate insulating and the gate electrode being covered by the conductive film 21; and

adding a second impurity 29 (Fig. 2C) to the semiconductor film while using the gate electrode and the sidewall as masks. Borel discloses the device/method is to be incorporated with CMOS structure manufacturing (Col. 1, lines 51-52); therefore, the device will inherently incorporate a logic circuit. Furthermore, channel lengths in CMOS technology were well below 2.0 μm (e.g., approaching 0.13 μm) at the time; therefore, Borel anticipates these claims.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 3 and 5-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Borel** (6,297,093 B1) in view of **Murai** (5,473,184).

Regarding claim 3:

Borel anticipates the method of claim 1 but **lacks** specifying whether or not the second impurity 29 (Fig. 2C) is added through the combined layers (the conductive film and the gate

insulating film). Murai is **cited only to show** it was very well known in the art that an impurity 7 can be added through a combination of two layers 2, 5 (note Figs. 2-3). Since Borel does not provide specifics regarding the second impurity, it would have been obvious to one of ordinary skill in the art to modify Borel by specifically reciting that the second impurity is added through the combined layers because Murai shows it was well known in the art to do so.

Regarding claims 5-8:

These claim are similar to claims 1-4 (addressed in detail above) except for the additional limitation for forming an insulating film over the gate insulating film and the gate electrode before forming the conductive film. Borel discloses all limitations within these claims **except for** the additional limitation. Murai **teaches** (in Figs. 1-2 and Col. 3, lines 43-46) that an insulating layer 5 formed over a gate insulating film 2 and a gate electrode 3 provides an effective etching stopping film during later etching processes. It would have been obvious to one of ordinary skill in the art to modify Borel by forming and insulating layer as taught by Murai because the insulating layer would serve as an effective etch-stopping layer during later processing steps. *Specifically regarding claim 7*: This claim is similar to claim 3 (addressed in detail above), i.e., Borel (in view of Murai) renders this claim obvious.

6. Claims 9, 10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Borel** (6,297,093 B1) in view of Papadas et al. (5,687,113; hereinafter, "**Papadas**").

Regarding claims 9, 10 and 12:

These claim are similar to claims 1, 2 and 4 (addressed in detail above) except for the additional limitations of removing the sidewall and the conductive film. Borel discloses

removing the conductive film 21 (note Fig. 2C); however, Borel **lacks** removing the sidewall. It is important to note that Borel incorporates Papadas by reference (see Borel, Col. 1, lines14-16 and Col. 2, lines 63-65). Papadas **teaches** (in Figs. 3C-3D and Col. 6, lines 49-52) sidewall removal before forming contacts is a matter of design choice, i.e., note Papadas specifies, "if desired, the spacer 29 near the source side is removed". Borel is essentially a modification of Papadas, wherein the modification lies in the addition of the conductive film 21 (note again, Borel, Figs. 2A-2B); and given Papadas' disclosure regarding sidewall removal, it would have been an obvious matter of design choice for one of ordinary skill in the art to modify Borel by removing the sidewall because Papadas specifies that such a removal is indeed a matter of choice.

7. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Borel** (in view of **Papadas**) as applied to claim 9 above, and further in view of **Murai** (5,473,184).

Regarding claim 11:

This claim is similar to claim 3 (addressed in detail above), accordingly, this claim is held obvious over the cited references with reasoning similar to that applied to claim 3 above.

8. Claims 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Borel** (in view of **Murai** (5,473,184) and **Papadas** (5,687,113).

Regarding claims 13-16:

These claims are similar to claims 5-12, i.e., independent claim 13 is essentially a combination of claims 5 and 9 (which were addressed in detail above). Borel discloses all

limitations in claim 13 **except** form forming an insulating film (over the gate insulating film and the gate electrode) and removing the sidewall. As explained in detail above, Murai **teaches** that an insulating film, formed over a gate insulating film and a gate electrode, will serve as an effective etch-stopping layer; and Papadas **teaches/shows** that sidewall removal is a matter of design choice (see above, "*Regarding claims 5-8*" and "*Regarding claims 9, 10 and 12*"). As explained above, it would have been obvious to one of ordinary skill in the art to modify Borel by incorporating an insulating layer (as taught by Murai) and by removing the sidewall (as taught by Papadas) because Murai teaches the insulating layer would provide an effective etch-stopping layer during later processing steps and Papadas teaches that sidewall remove is a matter of design choice.

9. Claims 21-23 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Liang** (6,180,502 B1) in view of **Papadas** (5,687,113).

Regarding claims 21-23 and 25:

Liang discloses (in Figs. 19-27 and Col. 9, beginning on line 24) a semiconductor manufacturing method, comprising the steps of:

forming a semiconductor film over a substrate, i.e., Liang discloses active region 402 (Fig. 19 and Col. 9, line 26-29); the active region would at least be a semiconductor region on the substrate; therefore, the active area could be referred to as a semiconductor film on the substrate;

forming a gate insulating film 407 on the semiconductor film;

forming a conductive film 410 on the gate insulating film;

forming a gate electrode 4200 (Fig. 25) on the conductive film, wherein the gate electrode has a length of about 0.18 μm (Col. 6, line 24), accordingly, the channel length will be approximately 0.18 μm;

adding a first impurity 430 (Fig. 24) to the semiconductor film through the conductive film 410 and the gate insulating film 407 while using the gate electrode as a first mask;

forming a sidewall 4400 to a side surface of the gate electrode in a condition of the gate insulating film 407 being covered by the conductive film (underneath the gate electrode 4200);

adding a second impurity 445 to the semiconductor film while using the gate electrode and the sidewall as masks (Fig. 27); and

processing the conductive film 410 while using the gate electrode as a second mask (Figs. 25-26 and Col. 10, lines 12-16).

Liang **lacks** removing the sidewall. Papadas **teaches** (in Figs. 3C-3D and Col. 6, lines 49-52) sidewall removal before forming contacts is a matter of design choice, i.e., note Papadas specifies, "if desired, the spacer 29 near the source side is removed". Therefore, it would have been an obvious matter of design choice for one of ordinary skill in the art to modify Liang by removing the sidewall because Papadas specifies that such a removal is indeed a matter of choice. *Specifically regarding claim 25:* Liang's disclosure is directed to integrated circuits (note Col. 1, beginning on line 12) the device would obviously incorporate a logic circuit.

Allowable Subject Matter

10. Claims 17-20 are allowable over the references of record.

11. Claim 24 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. The following is a statement of reasons for the indication of allowable subject matter:

Claims 17-20 and 24 are allowable primarily because claims 17 and 24 recite a limitation for adding the second impurity through the conductive film and the gate insulating film while using the gate electrode and the sidewall as masks. In other words, this limitation in combination as recited in claims 17 and 24 requires a portion of the conductive film to remain underneath the sidewall during the second impurity-addition step, where such an arrangement also requires the conductive film to be in contact with the gate electrode. The combination of process steps cannot be fairly suggested by the references of record.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The references listed on the attached Form PTO-892 (not specifically cited above) are cited to show methods incorporating conductive films that provide protection against damage due to plasma processes or ion-implanting process.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lex Malsawma whose telephone number is 571-272-1903. The examiner can normally be reached on Mon-Fri (6AM-2PM EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lex Malsawma

August 8, 2004

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